High-Aspect-Ratio Copper-Via-Filling for Three-Dimensional Chip Stacking

II. Reduced Electrodeposition Process Time

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Through-chip electrodes for three-dimensional packaging can offer short interconnection and reduced signal delay. Formation of suitable vias by electrodeposition into cavities presents a filling problem similar to that encountered in the damascene process. Because via dimensions for through-chip filling are larger and have a higher aspect ratio relative to features in damascene, process optimization requires modification of existing superconformal plating baths and plating parameters. In this study, copper filling of high-aspect-ratio through-chip vias was investigated and optimized with respect to plating bath composition and applied current wavetrain. Void-free vias 70 μm deep and 10 μm wide were formed in 60 min using additives in combination with pulse-reverse current and dissolved-oxygen enrichment. The effects of reverse current and dissolved oxygen on the performance of superfilling additives is discussed in terms of their effects on formation, destruction, and distribution of a CuI(III) thiolate accelerator.

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Three-dimensional (3D) chip stacking realizes high-density packaging and high-speed performance. High-aspect-ratio through-chip vias allow short interconnects and reduced signal delays.1-3 Copper has been selected as the through-chip electrode because of its compatibility with conventional multilayer interconnection in large-scale integration (LSI) and back-end processes.

A typical 3D packaging process proposed by ASET (Association of Super Advanced Electronic Technologies, Japan) includes the following steps: (1) formation of vias 70 μm deep by reactive ion etching (RIE); (2) formation of a SiO2 insulating layer; (3) deposition of a TiN barrier layer and a copper seed layer; (4) electrodeposition of copper inside the via; (5) formation of bumps followed by chemical mechanical polishing (CMP), polishing, and dicing of the wafer; and (6) multilayer stacking of chips connected through the copper vias.1-3 The via width is 10 μm, and the interconnection pitch is 20 μm. The minimum wafer thickness is 50 μm, and a 20 μm margin is required for polishing the wafer. Hence, a 70 μm depth is required for the through-chip electrode, and the via aspect ratio is 7.

Copper electrodeposition in high-aspect-ratio vias is one of the key technologies for 3D packaging. Voids or seams formed in the via may cause serious problems in reliability. An ASET Electronics SI Report published in 2000 (Ref. 4) cited results of via filling with 10 μm width and 70 μm depth. There were voids and seams in the via center. Sasaki et al.5 reported fabrication and electronic characterization of 3D chip-stacking technologies with through-chip vias 56 μm deep and 13 μm in diameter (aspect ratio 4.3). Unfortunately, the details of the electrodeposition process were not reported. In a previous study6 we succeeded in filling 70 μm vias by optimizing the additive composition and applying pulse-reverse current with an applied current density of \( I_{app} = 2.0 \text{ mA/cm}^2 \). The solution was made up of 130 g/L CuSO4·5H2O, 200 g/L H2SO4, 600 ppm polyethylene glycol (PEG), 100 ppm HCl, 5 ppm bis(3-sulfopropyl) disulfide (SPS), and increasing Janus Green B (JGB) concentration up to 20 to 50 mg/L. However, void and seam-free filling required 3.5 h.

In the 3D packaging process proposed by ASET, RIE and TiN barrier layer formation and copper seed layer formation require about 10 min. With a high-speed slurry, the CMP time can also be reduced to about 10 min. ASET simulated the process cost of their 3D packaging. If 3.5 h were required to fill the via, copper electrodeposition would be the rate determining step by a substantial margin, and so reduction of the electrodeposition time is required. The objective of this study was to reduce the electrodeposition time to 1 h to make this step compatible with the other operations.

Experimental

The chip pattern was reported previously.6-10 A chip with high-aspect ratio vias (70 μm depth and 10 μm width) was fabricated by a two-stage lithography and etching process, with the overhang removed in the second stage. The chip was then mounted on a rotating disk electrode (RDE) and immersed in the copper plating bath. The RDE rotation speed (RDE; Nikko Keisoku, motor speed controller, SC-5) was fixed at 1000 rpm, and a pulse-reverse current wavetrain (Power Supply HB-211 and BR-101B, Hokoto Denko) was applied. The pulse-reverse wavetrain is defined by three current values, a forward current \( I_{fwd} \), a reverse current \( I_{rev} \), and the off-time current \( I_{off} = 0 \), and by the corresponding time periods \( t_{fwd} \), \( t_{rev} \), and \( t_{off} \). After deposition, cross sections were cut and carefully polished to expose the via centers. The chip was first embedded in resin and cut with a step cutter (MC-170, Marto) to within about 100 μm before the via center. The remaining 100 μm was then removed by hand polishing, carefully guided by optical microscopy. The cross sections were then examined by field-emission scanning electron microscopy (FESEM) (model S-4300, Hitachi).

Table I shows the plating-bath composition and pulse-reverse plating conditions. The basic bath consisted of 200 g/L CuSO4·5H2O, 200 g/L H2SO4, and 100 g/L H2SO4. The additives included a proprietary suppressor (SPR) (0.5, 2, 5, or 10 mg/L) and leveler (LEV) (0.0, 0.2, or 0.5 mg/L) from EEJA (Electroplating Engineer of Japan), as well as SPS (1, 2, or 10 mg/L) and HCl (50, 70, or 150 mg/L). In a series of experiments at increasing forward current density, begin-
Table 1. Plating-bath composition and pulse-reverse current parameters.

<table>
<thead>
<tr>
<th>Additive</th>
<th>Concentration (g/L)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CuSO₄·5H₂O</td>
<td>200</td>
</tr>
<tr>
<td>H₂SO₄</td>
<td>25, 50, 75, 100</td>
</tr>
<tr>
<td>SPR</td>
<td>0.5, 1.0, 2.0, 5.0</td>
</tr>
<tr>
<td>LEV</td>
<td>0.2, 0.5, 1.0</td>
</tr>
<tr>
<td>HCl</td>
<td>50, 70, 150</td>
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<tr>
<td>SPS</td>
<td>1, 2, 10</td>
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Results and Discussion

Optimization of leveler concentration.— At forward current densities \( I_{on} = 4 \text{ mA/cm}^2 \), various LEV concentrations were tested in the range of 0.0 to 0.5 mg/L. Typical examples of via cross section micrographs are shown in Fig. 1 for LEV concentrations of 0.0, 0.2, and 0.5 mg/L with \( I_{on} = 4 \text{ mA/cm}^2 \) and a deposition time of 120 min. At a LEV concentration of 0.0 mg/L, there were large voids at the via center, and at 0.5 mg/L there were small and narrow voids. However, a LEV concentration of 0.2 mg/L produced no voids, and perfect via filling was achieved. With the optimized LEV concentration of 0.2 mg/L and applied current density of \( I_{on} = 4 \text{ mA/cm}^2 \), perfect via filling was achieved in 120 min.

Optimization of suppressor concentration.— The current density was increased to \( I_{on} = 5 \text{ mA/cm}^2 \), and various SPR concentrations in the range of 2.0 to 10.0 mg/L were tested. Typical examples of via cross-section micrographs are shown in Fig. 2 with SPR concentrations of 2.0 and 10.0 mg/L for deposition times of 90 min. SPR concentrations of 2.0 and 10.0 mg/L produced small voids at the center, as shown by the arrows. However, a concentration of 5.0 mg/L produced no void, and perfect via filling was achieved. With a SPR concentration of 5.0 mg/L and applied current density of \( I_{on} = 5 \text{ mA/cm}^2 \), perfect via filling was achieved in 90 min.

Figure 2. Micrographs of via cross sections formed with three different SPR concentrations. H₂SO₄, LEV, HCl, and SPS concentration is 100 g/L, 0.2 mg/L, 70 mg/L, and 2 mg/L, respectively. (a) 2 mg/L SPR; (b) 5 mg/L SPR; (c) 10 mg/L SPR.

Figure 3. Cyclic voltammetric stripping analysis. The normalized integrated stripping charge is plotted against SPR concentration at RDE rotation speeds of 100 and 1000 rpm.
Optimization of suppressor concentration by cyclic voltammetric stripping analysis.— Figure 3 shows the normalized CVS stripping area vs SPR concentration. The RDE rotation speed was 100 or 1000 rpm. To simulate the outside of the via, where the fluid velocity is relatively high, a rotation speed of 1000 rpm was used. To simulate the relatively low fluid velocity inside the via, a rotation speed of 100 rpm was used. If the normalized stripping area [area/area (at SPR = 0)] is larger for 100 rpm than for 1000 rpm, deposition is more rapid at the via bottom than the via outside, and bottom-up filling is expected. In Fig. 3, the difference in stripping area between 100 and 1000 rpm is largest at a SPR concentration of 5.0 mg/L. This concentration corresponds to perfect via filling as shown in Fig. 2.

Optimization of HCl, SPS, disulfide, and H2SO4 concentrations and pulse-reverse current parameters.— In addition to SPR and LEV, we also optimized the concentrations of HCl, SPS, and H2SO4. HCl was varied from 50 to 150 mg/L, H2SO4 from 25 to 100 g/L, and SPS from 1 to 10.0 mg/L. At this stage, we increased the current to 25 to 100 g/L, and SPS from 1 to 10.0 mg/L. Typical examples of via cross sections formed in the one-stage process with optimized HCl, SPS, and H2SO4 concentrations are shown in Fig. 4. Without O2 sparging, there is a small void at the via bottom (Fig. 6a; arrow). However, with O2 sparging there is no void, and perfect via filling is achieved. With O2 gas sparging, perfect via filling without any voids was achieved at \( I_{on} = 6 \text{ mA/cm}^2 \) and a deposition time of 75 min, produced no void, and perfect filling was achieved.

Two-step electrodeposition process.— The filling time was finally reduced to 60 min by application of a two-step deposition process with an initial current density \( I_{on} = 6 \text{ mA/cm}^2 \) for 50 min and a second higher current density \( I_{on} = 15 \text{ mA/cm}^2 \) for 10 min with O2 gas sparging throughout. Figure 7 shows the via cross section obtained by the two-step process; it produced no void and perfect filling was achieved.

Via cross section shapes with 50 min.— The key requirement for perfect via filling is an initial lower current of \( I_{on} = 6 \text{ mA/cm}^2 \) for 50 min with O2 gas sparging. Hence, we observed the via cross section with initial lower current of \( I_{on} = 6 \text{ mA/cm}^2 \) for 50 min without the second step. Figure 8 shows the via cross sections without O2 and with O2. Conformal electrodeposits were formed, and continuous seams from the via bottom to the top remained at the via center without O2 sparging. However, a clear V shape was formed and perfect via filling was achieved without any seam with O2 sparging. Formation of this clear V shape leads to perfect via filling. This bottom-up V-shape formation with O2 is very effective for shortening the electrodeposition time.

Mechanism of bottom-up filling with oxygen sparging.— Time-potential curves with O2 and N2 gas sparging are shown in Fig. 9. The electrodes are the simulated via outside (RDE) and via bottom (through-mask). A pulse-reverse current wavetrain was sparged into the plating solution and a pulse-reverse wavetrain with \( I_{on} = 6 \text{ mA/cm}^2 \) was applied. Figure 6 shows micrographs of via cross sections without and with O2 sparging. Without O2 sparging, there is a small void at the via bottom (Fig. 6a; arrow). However, with O2 sparging there is no void, and perfect via filling is achieved. With O2 gas sparging, perfect via filling without any voids was achieved at \( I_{on} = 6 \text{ mA/cm}^2 \) and a deposition time of 75 min, produced no void, and perfect filling was achieved.
applied. With O₂ gas sparging, the simulated via outside is at a more negative potential, and hence more inhibited than under N₂ sparging. However, no potential difference is observed for the simulated via bottom under O₂ or N₂ sparging.

In equilibrium with the metal, copper plating solutions contain a cuprous ion concentration in the millimolar range. Dissolved oxygen consumes the cuprous ion and removes the solution from equilibrium. Formation reactions of Cu(I)thiolate accelerator and oxidation reaction of Cu⁺ to Cu²⁺ are shown below

\[
2\text{Cu}^+ + 4\text{MPS} \rightarrow 2\text{Cu(I)thiolate} + \text{SPS} + 4\text{H}^+ \]  

\[
2\text{Cu}^+ + \frac{1}{2}\text{O}_2 + 2\text{H}^+ \rightarrow 2\text{Cu}^{2+} + \text{H}_2\text{O} \]

The distribution of these reactions in and around the via is illustrated in Fig. 10. The outside of the via is more accessible to dissolved oxygen than the via bottom, since the chip is rotated at 1000 rpm. The Cu(I)thiolate accelerator is thus readily oxidized to Cu²⁺ at the via outside (Eq. 2). Deep inside the via, transport of dissolved O₂ is impeded and accumulation of Cu(I)thiolate occurs. Hence, the Cu(I)thiolate is depleted at the via outside relative to the via bottom, and deposition is more inhibited there. Figure 10 illustrates the mechanism of the bottom-up via filling with O₂ sparging. Depletion of Cu(I)thiolate occurs at the via outside and accumulation of Cu(I)thiolate occurs in the via bottom. This inhibition and acceleration by Cu(I)thiolate accumulation results in the marked V-shaped via cross section observed in Fig. 8b.

Conclusions

Void-free filling of 70 μm deep and 10 μm wide vias was achieved by copper deposition with optimized additive concentrations, a pulse-reverse wavetrain, oxygen enrichment, and a two-stage process. Optimized proprietary additive concentrations of 5 mg/L SPR and 0.2 mg/L LEV produced void-free filling at 5 mA/cm² with a filling time of 90 min. The difference in normalized stripping area [Ar/Ar (SPR = 0)] detected by CVS at RDE rotation speeds of 100 and 1000 rpm shows the largest value at the optimum SPR concentration of 5 mg/L. SPS, HCl, and H₂SO₄ concentrations were optimized at a current density of I₀ = 6 mA/cm². The optimized concentrations are 2 mg/L SPS, 70 mg/L HCl, and 25 g/L H₂SO₄. The optimized pulse-reverse conditions were T₀ = T₉₀, T₁₀ = 200 ms; 10 ms; 200 ms and I₀ = I₉₀. However, at this composition small voids always formed at a current density of I₀ = 6 mA/cm². Perfect via filling was obtained with the optimized plating bath with I₀ = 6 mA/cm² and 75 min by sparging with O₂. The effect of O₂ gas is interpreted to result from oxidation of a Cu(I)thiolate accelerant preferentially at the outside of the vias. Finally, a two-step electrodeposition process consisting of initial lower current of I₀ = 6 mA/cm² for 50 min and second higher current of I₀ = 15 mA/cm² for 10 min was applied, resulting in perfect via filling within 60 min. A clear, bottom-up V-shape-formed via cross section was observed after the initial lower current of I₀ = 6 mA/cm².

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