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Development of Cu-Core Pb-Free Solder Bumps

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Cu-core Pb-free solder bumps were developed by electrodeposition in combination with photolithography. A bump with a pitch of 100 μm and a diam of 50 μm was successfully achieved with dry film resist (80 μm thick) under optimum process conditions, and the bumps reached the target height of 50 ± 5 μm. The adoption of a dummy pattern improved the height uniformity of the bumps. Pull test results showed that the shear strength of the Cu bump (around 45 gf) was obtained by the soft-etching pretreatment of the Cu foil surface. Sn-Zn, Sn-Ag, Sn-Cu, and Sn-Bi platings were deposited as Pb-free solders with near-eutectic compositions. In particular, the interface properties of Sn-Zn solder plating/Cu were investigated after reflowing in this study, as well as the effect of Ni plating as an under ball metallurgy layer on compound formation at the interface. It was found that a compound of Υ-Cu_5Zn_8 layer existed in the interface of the reflowed Sn-Zn plating/Cu. The Ni plating layer inhibited the formation of the interface Υ-Cu_5Zn_8 compound with reflowing.
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The trend of electronic devices toward being high performance, downsize, and lightweight requires an interconnection technology of high density such as a flip chip package which is suitable for high input/output numbers, and packaging miniaturization in the electronic industry.[1,2] The fabrication of solder bumps is a critical step in the technology of high-density bonding, and it is usually performed with low-cost screen printing. However, with the resolution limitation, this method cannot meet the requirement on preparing fine solder bumps. Electrodeposition is a very attractive technique used recently in the formation of solder bumps with small size and fine pitch.[3-8]

Our project aimed to develop Cu-core Pb-free solder bumps for application in high-density interconnections by electrodeposition combined with photolithography. The adoption of the Cu core is to prevent the deformation of solder during the reflow process, in addition to its advantages of thermal and electrical conductivity. Also, there are increasing demands for Pb-free products in the electronics industry worldwide because of the detrimental effects of Pb element in the environment.[9-13] Additionally, soft errors caused by alpha particles emitted from Pb in solder bumping are also of special concern in high-density interconnections.[14] Thus, Pb-free solders are currently receiving much interest in the field of electronic interconnection.

This study was intended to attach a layer of Pb-free plating on the surface of a Cu core bump to make it a Cu-core Pb-free solder bump. In this work, the Cu bump preparation was studied with pattern electroplating, and the height uniformity and the shear strength of the Cu bump were discussed as well. Sn-Zn, Sn-Ag, Sn-Cu, and Sn-Bi platings were deposited as Pb-free solders, and an investigation was carried out on the interface property of reflowed Sn-Zn plating/Cu.

Experimental

Bump patterns were formed on dry film resist (DFR) that was laminated on Cu foil, and then Cu plating and lead-free plating were sequentially deposited into the pattern. Finally, Cu core-solder bumps were obtained by removing the DFR. Figure 1 presents the preparation process of Cu core-solder bump. The DFR (80 μm thick-ORDYL MP100, TOK Co. Ltd.) was employed for the fabrication of bump patterns with a pitch of 100 μm and a diam of 50 μm. A negative photo mask was adopted during the process of photolithography, as shown in Fig. 2. A dummy pattern, which included dummy lines around the pattern (841 holes), was also attempted to improve the uniformity of bump height.

A polarization test of the patterned Cu foil was performed with an HZ-3000 automatic polarization system (Hokuto Denko, Co. Ltd.), and a saturated calomel electrode (SCE) was used as reference electrode. The depositions of Cu bump and Pb-free solder were conducted by the galvanostatic method at room temperature (Hokuto Denko, Co. Ltd. potentiostat/galvanostat HA-151). Figure 3 shows the experimental device. A commercial Cu plating bath (OPC high purity Cu plating bath, Okuno Chemical Industries Co. Ltd.) with additives was used in the Cu bump deposition. This bath composition was similar to that of the basic bath (1.85 M H_2SO_4, 0.6 M $CuSO_4 \cdot 5H_2O$) used in our lab; the additives included Cl^- (50 mg/L) and a brighter agent (20 mL/L) from Uemura Industry Co. Ltd. The cathode current density was 15-30 mA/cm^2 during the process of electrodeposition, and a Cu plate served as an anode.

The cathode current density was 20-40 mA/cm^2 during the depositions of Sn-Zn, Sn-Cu, Sn-Bi, and Sn-Ag plating on Cu, and the Sn plate served as an anode. The plating baths of Pb-free solder were from Ishihara Chemical Co. Ltd. (Sn90/10Zn, Sn99.3/0.7Cu, Sn95/5Bi, Sn96.5/3.5Ag). The composition of the Pb-free plating layer was analyzed by energy dispersive X-ray analysis. Ni plating was deposited as an under ball metallurgy (UBM) layer at the interface of the Sn-Zn plating/Cu foil with the bath of Ni plating. The cathode was rotated at 300 rpm during the electrodeposition processes.

The height of the Cu bump was measured by the laser detection method. The shear strength of the bump was examined by the pull test (bond tester 2400A, Dage Precision Industries).

The Sn-Zn plating layer on Cu foil was reflowed in a vacuum furnace for 1 min at a peak temperature of 229°C. The rate of the temperature increase was 16.7°C/min. The morphology of the Cu bump was observed by scanning electron microscopy (SEM, JEOL, JSM-5500s), and the interface microstructure of the reflowed Sn-Zn plating/Cu sample was observed by field-emission-scanning electron microscopy (FE-SEM, Hitachi, S-4300) and transmission electron microscopy (TEM, Hitachi, H-700H). The element depth profile of this reflowed sample was analyzed by glow discharge spectrometry (GDS, Horiba, JY-5000RF).

Results and Discussion

Cu bump preparation.—DFR was better than spin-coating resist in forming a thicker pattern on Cu foil. The 80 μm thick DFR showed good resolution which ensured the achievement of patterns with a pitch of 100 μm. The DFR could be removed by alkaline solution. Table I gives optimum parameters for the photolithography process of DFR. A fine pattern was obtained on Cu foil under these conditions, as seen in Fig. 4.

Polarization tests were carried out on this patterned Cu foil electrode and the plate Cu foil electrode in the Cu plating bath at room temperature with a scan rate of 20 mV/s. The results are illustrated in Fig. 5. The polarization curve of the patterned sample shows a diffusion limitation region where the current density (about 63 mA/cm^2) does not change in the potential range around 0.5-0.9 V

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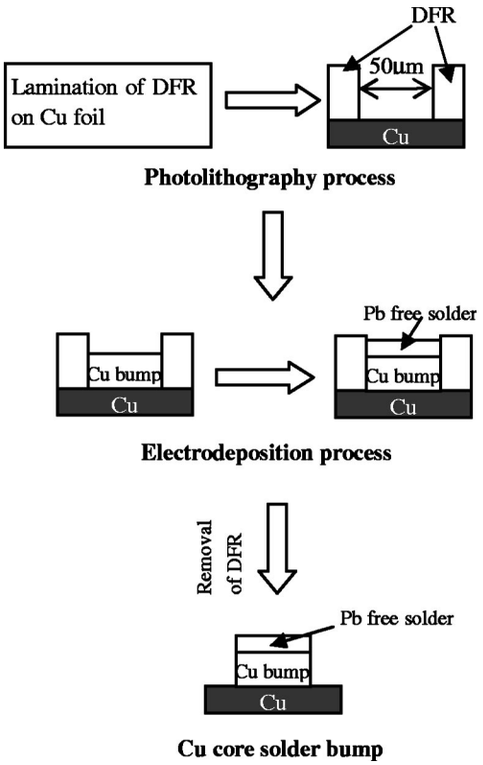


Figure 1. Flow diagram of preparation processes for Cu-core Pb-free solder bumps.

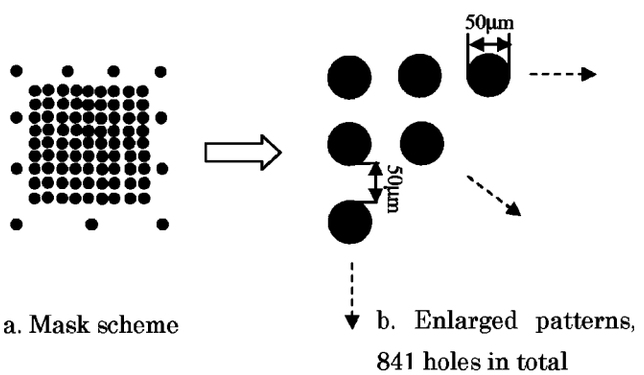


Figure 2. The scheme of photo mask used in photolithography process.

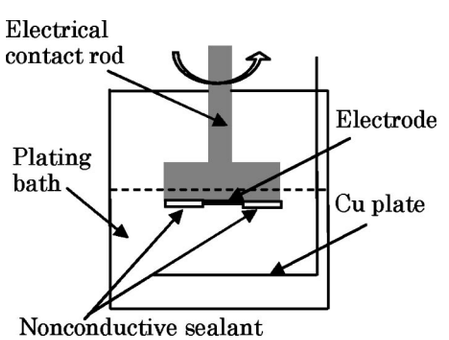


Figure 3. Schematic diagram of rotation cathode.

Table I. Photolithography parameters of 80 μm thick DFR.

Exposure time	Developing bath	Developing temperature	The time of shower developing	Developing pressure
4 s	1 wt % Na_2CO_3	50 ± 3°C	6 min	5 kgf/cm^2

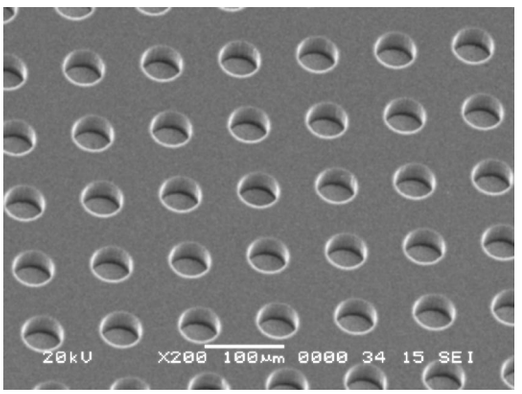


Figure 4. The morphology of the pattern formed on Cu foil.

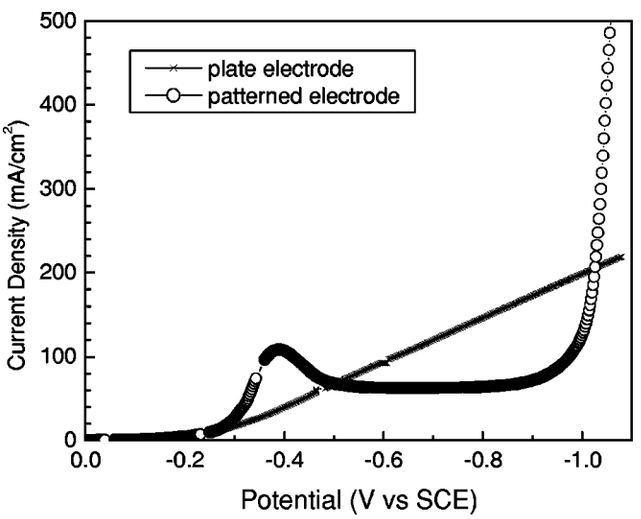


Figure 5. Polarization curves of patterned and plate Cu foil electrodes in Cu plating bath, 300 rpm, with scan rate 20 mV/s.

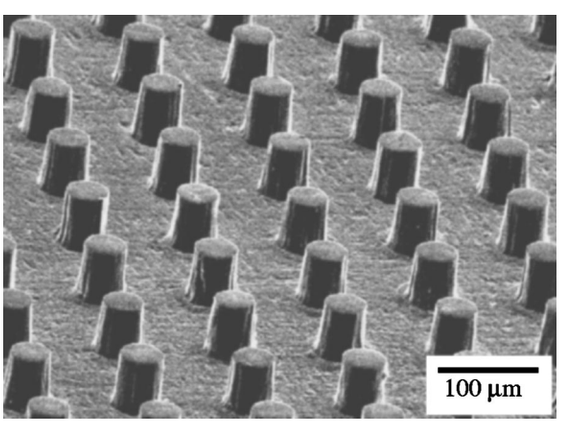


Figure 6. The morphology of Cu bump prepared with the pattern on 80 μm thick DFR (SEM).

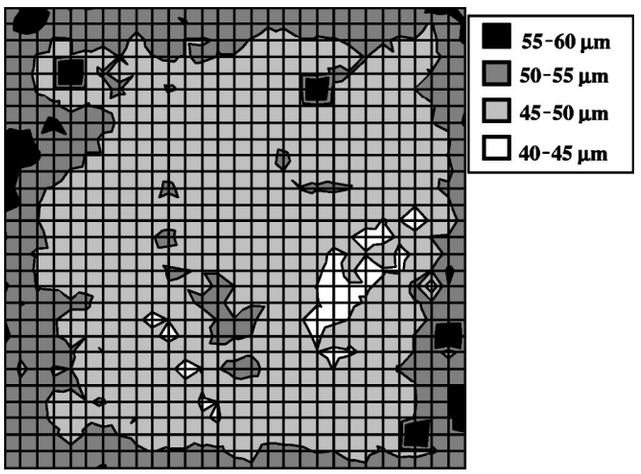


Figure 7. Distribution map of Cu bump height (bumps prepared with the pattern on 80 μm thick DFR).

(*vs.* SCE). However, there is no such limiting current density up to the potential of 1.0 V (*vs.* SCE) in the polarization of the plate electrode. Evidently, this phenomenon is due to the mass-transfer limitation of copper ion caused by the high aspect pattern.

However, for the patterned electrode, there is a wide current regime of Tafel reaction before reaching the limiting current density of 63 mA/cm^2 according to the polarization curve. So, the current density of 15-30 mA/cm^2 located in the Tafel region was applied in Cu electrodeposition. The Cu deposition reaction on the patterned electrode was not affected by the mass-transfer limitation of copper ion in this study.

Cu bump preparation was completed successfully with the previously described patterned Cu foil and the removal process of DFR (MP removal bath, 40°C, TOK Co. Ltd.). Figure 6 shows the images of uniform Cu bumps with a pitch of 100 μm and a diam of 50 μm. The smooth surface of the Cu bump, which was attributed to the additives' effects in the Cu plating bath, made it more accurate to measure the bump height by laser detection.

The test results for the bump height (841 bumps) are shown in Fig. 7. Generally, the bumps around the circumference of the pattern are relatively high in the whole distribution map of height. This is attributed to the concentration of cathode current around the pattern.

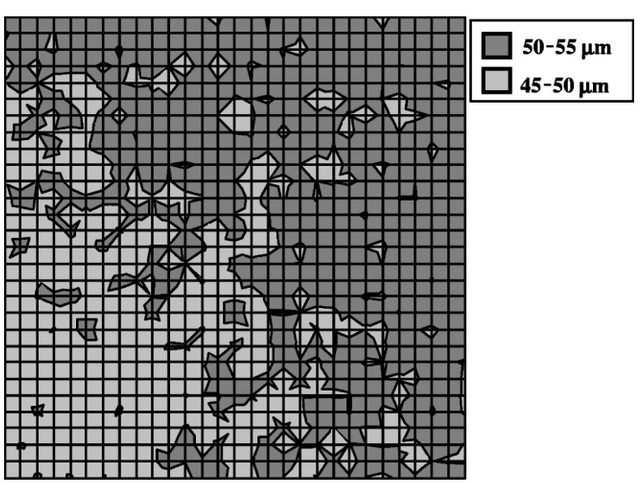


Figure 8. Distribution map of Cu bump height (bumps prepared with the dummy pattern on 80 μm thick DFR).

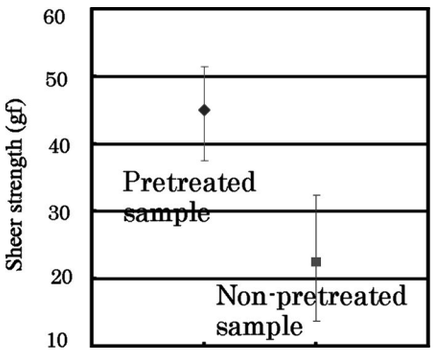


Figure 9. Shear strength of Cu bump with/without soft-etching pretreatment.

However, the bumps almost reach the height of 45-55 μm aimed for the solder bump, even though the height uniformity needs to be further modified for all bumps.

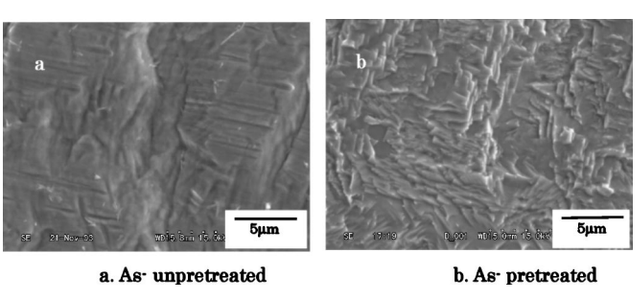
Figure 8 shows the heights of the bumps that were obtained by a modified pattern with 4 dummy lines around the pattern (841 holes). In this case of the dummy pattern, all bump heights are located in the range of 45-55 μm. So, 100% of bumps with a height of 50 ± 5 μm was achieved by this dummy pattern. The dummy lines around the pattern modified the distribution of cathode current on the pattern surface and made the deposition of Cu on the pattern more uniform. The height uniformity of the bumps is effectively improved by the dummy pattern.

Shear strength of Cu bump.—The surface of the Cu foil was treated by a soft-etching bath at 25°C for 3 min and acid cleaning at 40°C for 3 min before Cu electrodeposition to improve the shear strength of the Cu bumps. This kind of soft-etching bath was a sodium supersulfated solution from Uemura Industry Co. Ltd. Figure 9 shows measurement results of samples with/without the soft-etching pretreatment.

It is seen that the shear strength of the pretreated sample, around 45 gf, is twice that of the sample without the pretreatment. This can be attributed to the surface roughening of Cu foil with the pretreatment, which improved the adhesion of Cu bumps on Cu foil, as shown in Fig. 10. Soft-etching pretreatment plays a role in increasing the shear strength of Cu bumps.

Pb-free solder plating.—Pb-free plating was electrodeposited sequentially on the Cu bumps (see the electrodeposition process in Fig. 1). Figure 11 shows the morphology of Cu core bumps with Pb-free plating of Sn-Zn.

The composition of the Pb-free plating is given in Table II. The analysis results indicate that near-eutectic Pb-free alloys (excluding Sn-Bi alloy) which were expected to be used as solder materials



a. As- unpretreated b. As- pretreated

Figure 10. The morphology of Cu foil surface before/after the soft-etching pretreatment (FE-SEM).

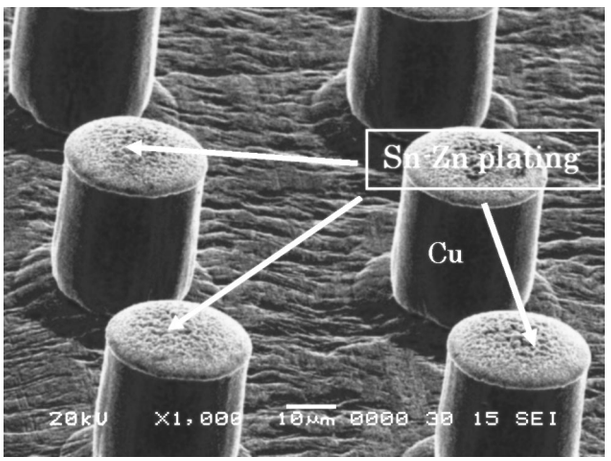


Figure 11. The morphology of Cu bumps with Sn-10 wt %Zn plating (SEM).

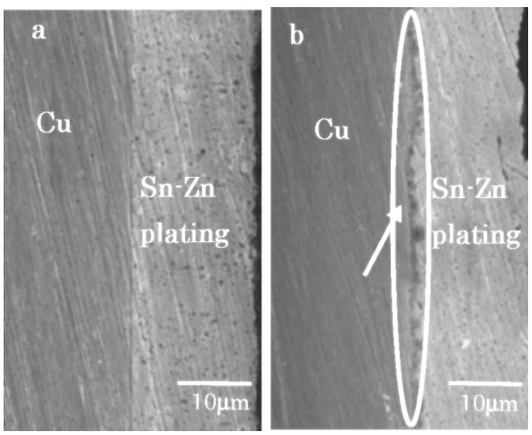


Figure 12. Cross-sectional morphology of Sn-10 wt %Zn plating/Cu (FE-SEM): (a) as deposited and (b) reflowed.

were obtained. The melting point of Sn-10 wt %Zn plating is the lowest among these four kinds of plating,[15] making it a promising material for low-temperature solder.[16,17]

The interfacial property of the reflowed Sn-Zn plating/Cu foil was primarily investigated in this work, as seen in Fig. 12. A dark layer (indicated by the arrow in Fig. 12b) appears at the interface of the reflowed Sn-Zn plating/Cu. This is considered to be interface reaction layer caused by the active element of Zn diffusing to the interface during reflow, as reported for a Sn-Zn solder ball/Cu substrate.[16,18] GDS analysis clarified the element distribution in the reflowed Sn-Zn plating/Cu, as indicated in Fig. 13. It is found that there exists an interface region composed of elements of Cu, Sn, and Zn between Sn-Zn plating and Cu, which could be due to the diffusions of elements during reflow. The Zn peak is especially significant compared with its content in the bulk of the Sn-Zn plating layer. It means that the content of active Zn clearly increases at the interface region with reflowing. Accordingly, it is reasonable that compounds were formed because of reactions among these elements diffusing to the interface region during the process of reflowing, in particular, in consideration of active Zn diffusion to the interface.

TEM observation provided a further analysis on the interface microstructure of reflowed Sn-Zn plating/Cu, as seen in Fig. 14. It shows more clearly the interface layer, which consisted of Υ-Cu_5Zn_8 compound predominantly according to the diffraction pattern. This result confirms that a Cu-Zn compound was formed at the interface of Sn-Zn plating/Cu with the reflow at 229°C.

The reaction layer affects joint reliability because the Cu-Zn compound layer is unstable, and an interface reaction can proceed at high temperature.[16] Here, we attempted to attach Ni plating on the interface between Cu and Sn-Zn plating as a barrier layer to prevent Υ-Cu_5Zn_8 compound formation. Figure 15 gives the interface morphology of the reflowed Sn-Zn plating/Ni plating/Cu. The result shows that, with Ni plating at the interface of the reflowed Sn-Zn plating/Cu, no reaction layer like the one that appeared in the case without Ni plating (see Fig. 12b) exists at the interface. It is indicated that Ni plating plays a role in inhibiting the formation of the interface layer during reflowing. As seen in the GDS analysis

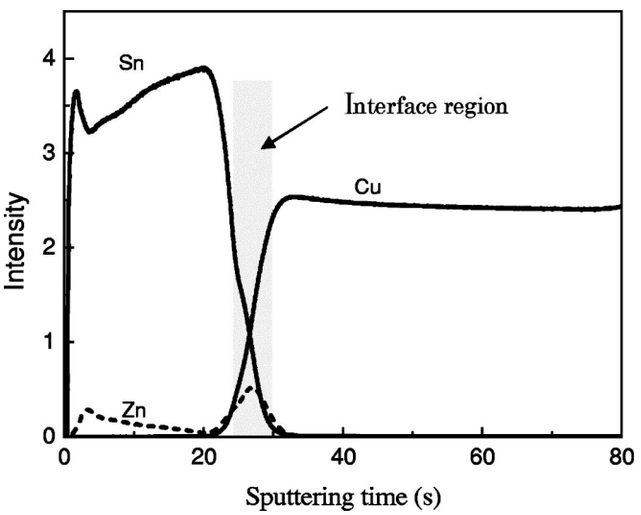


Figure 13. The element distribution in reflowed Sn-10 wt %Zn plating/Cu (GDS).

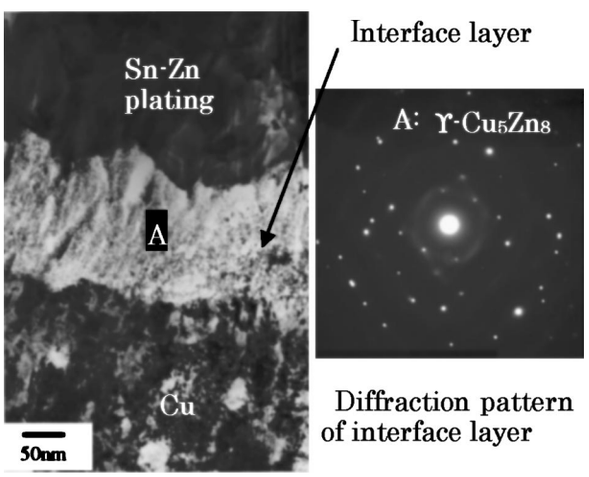


Figure 14. Interface microstructure of reflowed Sn-10 wt %Zn plating/Cu (TEM).

Table II. The composition of Pb-free plating.

Solder plating	Sn/Cu	Sn/Ag	Sn/Zn	Sn/Bi
Alloy contents (wt %)	1.3	3.3	10.5	5.0

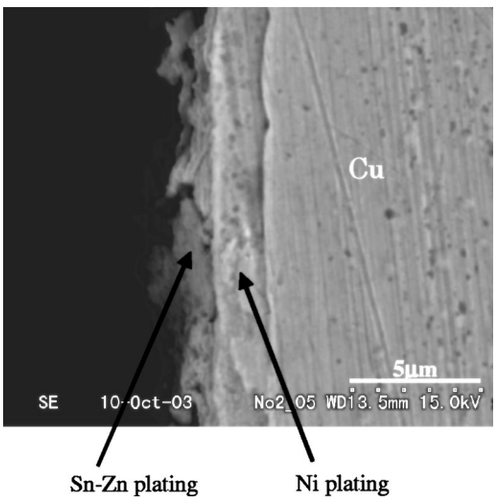


Figure 15. Cross-sectional morphology of reflowed Sn-10 wt %Zn plating/Cu with Ni plating at its interface (FE-SEM).

(Fig. 16) of the reflowed Sn-10 wt %Zn/Ni/Cu, no Zn peak exists at the interface region where Ni plating is predominant. Ni plating served as a barrier layer to Zn diffusion to the interface during reflow. As a result, the Zn-Cu compound would not be formed at the interface of reflowed Sn-10 wt %Zn/Cu with a Ni UBM layer.

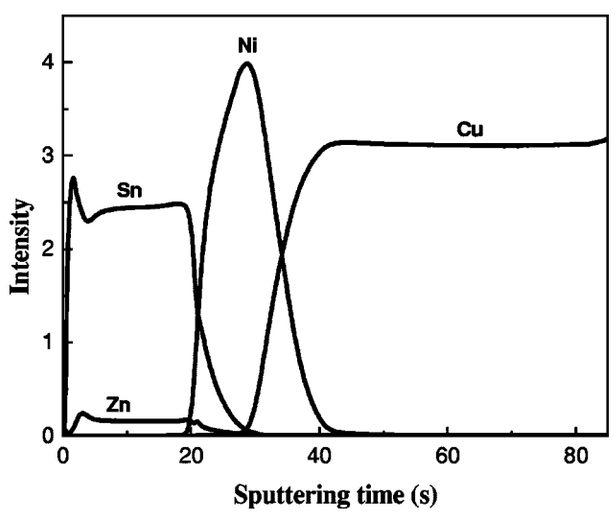


Figure 16. The element distribution in reflowed Sn-10 wt %Zn plating/Cu with Ni plating at its interface (GDS).

Conclusions

1. Cu core solder bumps with a pitch of 100 μm and a diam of 50 μm were successfully prepared by an electrodeposition method combined with a photolithography technique.

2. Uniform bumps with a height of 50 ± 5 μm were achieved with 80 μm thick DFR. The height uniformity of the bumps was further improved by using a dummy pattern.

3. A reaction layer consisting of a Υ-Cu_5Zn_8 compound was formed at the interface of the reflowed Sn-10 wt %Zn plating/Cu. Ni plating, which served as a UBM layer, played the role of barrier to the formation of a reaction layer at this interface.

Acknowledgments

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References

1. K. N. Tu and K. Zeng, *Mater. Sci. Eng., R.*, **34**, 1 (2001).
2. E. Hayashi, S. Wakiyama, K. Harada, S. Baba, T. Ozawa, A. Maeda, and M. Kimura, in *2003 International Conference on Electronics Packaging Proceedings*, IEEE CPMT, IMPS Japan, and JIEP, p. 465 (2003).
3. K. Kondo, K. Fukui, K. Uno, and K. Shinohara, *J. Electrochem. Soc.*, **143**, 1880 (1996).
4. K. Kondo, K. Fukui, M. Yokoyama, and K. Shinohara, *J. Electrochem. Soc.*, **144**, 466 (1997).
5. K. Kondo and K. Fukui, *J. Electrochem. Soc.*, **145**, 840 (1998).
6. S. Arai, Y. Funaoka, N. Kanako, and N. Shinohara, in *Proceedings of the 7th Symposium on Microjoining and Assembly Technology in Electronics*, Yokohama, p. 269, Japan Welding Society (2001).
7. B. Kim and T. Ritzdorf, *J. Electrochem. Soc.*, **150**, C53 (2003).
8. K. Lin and Y. Liu, *J. Electrochem. Soc.*, **150**, C529 (2003).
9. S. Arai, N. Kaneko, and T. Watanabe, *Mater. Trans., JIM*, **39**, 439 (1998).
10. F. Zhang, M. Li, B. Balakrisnan, and W. T. Chen, *J. Electron. Mater.*, **31**, 1256 (2002).
11. C. B. Lee, S. J. Suh, Y. E. Shin, C. C. Shur, and S. B. Jung, in *Proceedings of the 8th Symposium on Microjoining and Assembly Technology in Electronics*, Yokohama, p. 351, Japan Welding Society (2002).
12. M. Kitajima, T. Shono, T. Ogino, T. Kobayashi, K. Yamazaki, and M. Noguchi, in *2003 International Conference on Electronics Packaging Proceedings*, IEEE CPMT, IMPS Japan, and JIEP, p. 339 (2003).
13. C. W. Hwang, K. Suganuma, M. Kiso, and S. Hashimoto, in *Proceedings of the 13th Microelectronics Symposium*, Osaka, p. 37, JIEP (2003).
14. M. W. Roberson, P. A. Deane, S. Bonafede, A. Huffman, and S. Nangalia, *J. Electron. Mater.*, **29**, 1274 (2000).
15. T. B. Massalski, H. Okamoto, P. R. Subramanian, and L. Kacprzak, *Binary Alloy Phase Diagrams*, 2nd ed., ASM International, Metals Park, OH (1990).
16. K. Suganuma, Books series 159: Technologies of Lead Free Soldering, Industry Committee (2000).
17. M. Kitajima and T. Shono, *J. Jpn. Inst. Electron. Packag.*, **6**, 380 (2003).
18. H. Yanagawa, T. Imamura, E. Ide, A. Hirose, and K. Kobayashi, in *Proceedings of the 12th Microelectronics Symposium*, Osaka, p. 191, JIEP (2002).