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Improvement of Detectability for CMOS Floating Gate Defects in Supply Current Test

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Abstract

We already proposed a supply current test method for detecting floating gate defects in CMOS ICs. In the method, increase of the supply current caused by defects is promoted by superposing a sinusoidal signal on the supply voltage. In this study, we propose one way to improve detectability of the method for the defects. They are detected by analyzing the frequency of supply current and judging whether secondary harmonics of the sinusoidal signal exists or not. Effectiveness of our way is confirmed by some experiments.

1. Introduction

It is well known that there exist many floating gate defects which can not be always detected by functional test methods based on stuck-at fault models[1],[2]. It has also been shown that some of them cannot be detected even by I_{DDQ} test method[1]-[4]. It has therefore become an earnest request for test engineers to develop powerful test methods for such defects.

From the background mentioned above, Hashizume et.al. proposed a supply current test method with an externally applied sinusoidal electric field[5]. It intends to excite the defective node with the electric field so that some abnormal supply current flows. We also proposed a supply current test method in which the floating node is excited by a sinusoidal signal superposed on the supply voltage[6]. By the use of either method, we can detect existence of some defects with the supply current increase caused by conduction of a defective transistor in a DUT. It seems however that we cannot expect so much high detectability, if the conduction occurs marginally in the DUT. In this study, we try to improve the detectability for such defects.

In the two test methods mentioned above, the supply current of defect-free DUT contains some amount of the same frequency component as the externally applied sinusoidal electric field or the superposing sinusoidal signal on power voltage, however scarcely contains the harmonics component. On the other hand, if the defective transistor conducts marginally, the supply current will contain a large amount of harmonics, especially, secondary one. From such a point of view, we analyze the supply current by a spectrum analyzer and estimate existence of the defect by the ratio of the secondary harmonics to the fundamental frequency component.

In the next section, we describe the test method[6] for the study. In the succeeding section, we propose a new way for detecting the floating gate defects in CMOS ICs. In the fourth section, the validity of the way is confirmed by some experimental examinations for three CMOS NAND gates.

Finally, we conclude with a summary and our future works.

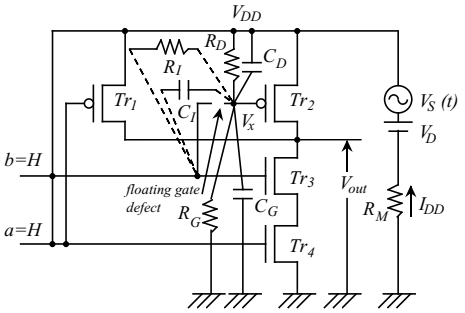

Figure 1. Test circuit for NAND gate with a floating gate defect

2. Test circuit and power supply current

2.1. Test Circuit

In our test method, an AC component is superposed on DC power supply[6]. Figure 1 shows the test circuit attached to a NAND gate. V_D and $V_S(t)$ represent DC power supply voltage and sinusoidal supply voltage, respectively. Suppose that there exists a floating gate defect of p-MOS transistor Tr_2 as shown in the figure. C_D, C_G and C_I are stray capacitances from the floating node to the power supply source, the ground (GND) and the input terminal for the input b, respectively. R_D, R_G and R_I are leakage resistances defined in the same way. Both the input terminals are connected to the power supply node so that a conductive path through Tr_2 may be constructed. Existence of the defect can be detected as increase of the current passed through resistor R_M.

2.2. Bound of power supply voltage

Let us define V_{DD} and $V_S(t)$ in Figure 1 by

$$V_{DD} = V_D + V_S(t) \tag{1}$$

$$V_S(t) = A \sin \omega t \tag{2}$$

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where A and ω are the amplitude and the frequency in the sinusoidal supply voltage, respectively. The maximum of V_{DD} is bounded to the maximum rating voltage V_{MAX} of the DUT. Then, V_D and A must satisfy the following inequality.

$$V_D + A < V_{MAX} \tag{3}$$

On the other hand, the minimum of V_{DD} must be at least a level at which the conductive path for the test can be constructed. In case of Figure 1, this condition results in the inequality,

$$V_D - A > |V_{tp}| \tag{4}$$

where V_{tp} is the threshold voltage of p-MOS transistor(Tr_2).

If we keep V_D to $(V_{MAX} + |V_{tp}|)/2$, the maximum value of applicable AC component is $(V_{MAX} - |V_{tp}|)/2$. The higher or the lower we keep it than $(V_{MAX} + |V_{tp}|)/2$, the lower the value of the applicable AC component becomes, because the highest value and the lowest value of AC component are restricted from the inequalities (3) and (4), respectively.

If the defective transistor is n-MOS type, we only have to change V_{tp} in the inequality (4) to V_{tn}, where V_{tn} is the threshold voltage of n-MOS transistor.

2.3. Analysis of supply currents

Suppose that a DUT is the same type of NAND gate as Figure 1 and defect-free. If both inputs are connected to V_{DD}, the equivalent circuit can be shown in Figure 2, where C is the total stray capacitance existing in parallel with the power supply source except C_G. In the same way, R is defined as the total leakage resistance existing in parallel with the power supply source except R_G. If the value of R_M is

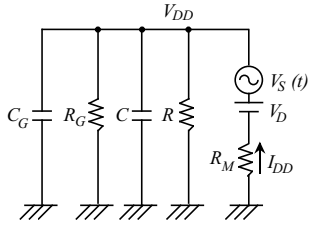


Figure 2. Equivalent test circuit for a defect-free NAND gate

enough small in comparison with the total impedance of the NAND gate, the current I_{CN} which flows through C and C_G is given as follows.

$$I_{CN} = \omega A(C + C_G)\cos\omega t \tag{5}$$

In the same way, the current I_{RN} which flows through R and R_G is given as follows.

$$I_{RN} = (\frac{1}{R} + \frac{1}{R_G})(V_D + A\sin\omega t) \tag{6}$$

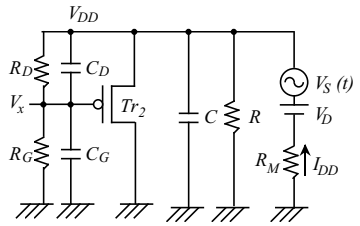


Figure 3. Equivalent test circuit for the defective NAND gate

Then, the supply current I_{DDN} is given by

$$I_{DDN} = I_{CN} + I_{RN} \tag{7}$$

Notice that I_{DDN} contains only the same frequency component as $V_S(t)$.

If the transistor Tr_2 in the same DUT has a floating gate defect, the equivalent circuit for the test is shown by Figure 3. C_I and R_I are merged into C_D and R_D, respectively. Thus, we exclude them in the succeeding description.

The potential V_x of the defective node can be approximated to the following equation.

$$V_x = \frac{AC_D}{C_D + C_G}\sin\omega t + \frac{R_G}{R_D + R_G}V_D \tag{8}$$

If the value of V_x becomes lower than $V_{DD} - |V_{tp}|$ even in a moment, some amount of source to drain current I_T flows. Hence, the supply current I_{DDF} through R_M in such the condition is shown by the following equations.

$$I_{DDF} = I_{CF} + I_{RF} + I_T \tag{9}$$

$$I_{CF} = \omega A(C + \frac{C_D C_G}{C_D + C_G})\cos\omega t \tag{10}$$

$$I_{RF} = (\frac{1}{R} + \frac{1}{R_D + R_G})(V_D + A\sin\omega t) \tag{11}$$

We can analyze I_{DDF} for an n-MOS transistor in the same way and obtain the same equations as above. In order that the defect is detectable from the level of I_{DD}, the magnitude of I_T must be enough lager than that of $I_{CN} + I_{RN}$, because $I_{CN} \simeq I_{CF}$ and $I_{RN} \simeq I_{RF}$.

3. Improvement of detectability

It is clear from the equations(5)∼(7) that I_{DDN} contains a small amount of the AC leakage component of frequency ω. If the DUT has the defect as shown in Figure 1, and the value of V_x is in the active region of Tr_2 during all over the phase of the sinusoidal component ω, the source to drain current of Tr_2 also flows during all over the phase. Hence, it seems that both AC and DC components in I_T become large in comparison with the corresponding ones in I_{DDN}. Figure 4 shows schematically the relation between V_x and I_T in such a situation. As the increase of I_T results in that of the current through R_M, we can easily detect the defect by observing the average or the peak of I_{DD}.

If the value of V_x is in a range such that it brings Tr_2 into the active region only in some restricted duration of the

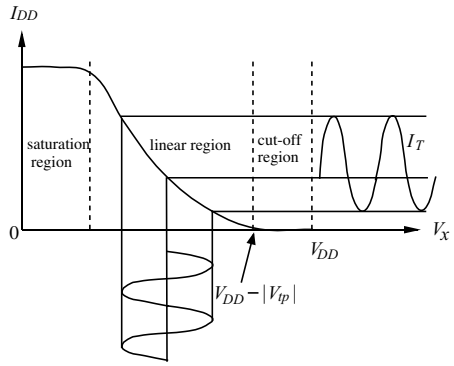


Figure 4. Relation between V_x and I_{DD} with dynamic behavior of a defective p-MOS transistor; case that Tr_2 is fully on state

phase in $V_S(t)$, that is Tr_2 is excited marginally, the source to drain current flows intermittently only in the same duration. Figure 5 shows schematically such a current. The

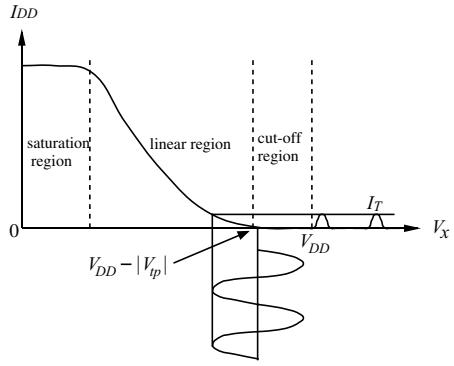


Figure 5. Relation between V_x and I_{DD} with dynamic behavior of a defective p-MOS transistor ; case that Tr_2 is intermittently on-state

waveform of I_T is non-sinusoidal. Our method can detect the defect even in such a situation as long as the average or the peak of I_{DDF} is enough large in comparison with that of I_{DDN}. However, if the magnitude of I_{DDF} is so small that the conventional current test method cannot detect it, it may not be easy to detect it by the current increase even in our test method. One way to overcome the difficulty is to analyze the waveform of I_{DD} in the following way.

As mentioned above, I_{DDN} contains only one frequency component(ω). On the contrary, I_{DDF} contains not only ω component but also its harmonics, especially 2ω component, if the defective transistor conducts marginally, because the waveform of the I_T becomes a series of clipped sinusoidal waves. It is therefore expected that we can detect it more sensitively by means of frequency analysis of

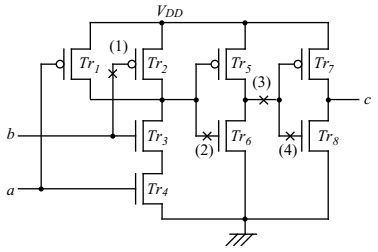


Figure 6. Locations of defects

I_{DD}.

From the equations (5) and (10), the magnitudes of both I_{CN} and I_{CF} increase with increase of the frequency ω, while the magnitude of I_T scarcely increases both in its peak and average, even if it increases. Hence, the lower the frequency ω becomes, the easier the defect detection by current level becomes. This is also valid for the way of harmonics detection. On the other hand, it is desirable to raise ω high from the view point of test speed. It seems therefore better that we decide the value of ω on compromise between the two factors mentioned above.

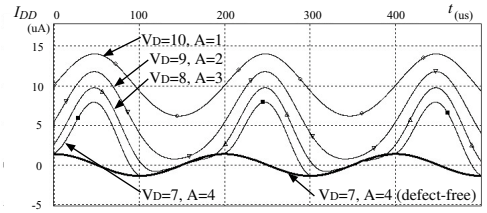
4. Experimental results

For the purpose of the experimental examination, we picked up three NAND gate packages TC4011BPs($V_{MAX} = 18(V)$, $V_{tp} = -1.0(V)$, $V_{tn} = 1.0(V)$) manufactured by Toshiba Co.. Each of them has four 2-inputs NAND gates. We made up only one floating gate defect per package. The defect of each DUT is different from the others. Figure 6 shows the locations of the defects by marking crosses (1)-(3) on a CMOS NAND circuit. They were caused by cutting the corresponding aluminum wires with an FIB (Focused Ion Beam).

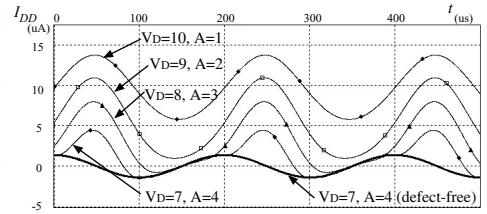
Figure 7(a),(b) and (c) show the waveforms measured from the DUTs corresponding to the defects(1),(2) and (3) shown in Figure 6, respectively. A waveform for a defect-free DUT is also added in each figure for a reference. Sum of V_D and A in each DUT was kept constant so that the peaks of V_{DD}s for all the curves of each DUT coincided with each other.

defect no.	V_D	A	spectrum ratio	
			defective DUT	defect-free DUT
(1)	10	1	0.043	0.019
	9	2	0.186	0.009
	8	3	0.435	0.007
	7	4	0.813	0.009
(2)	10	1	0.063	0.019
	9	2	0.174	0.009
	8	3	0.250	0.007
	7	4	0.375	0.009
(3)	6	1	0.833	0.017
	5	2	0.564	0.018
	4	3	1.750	0.023

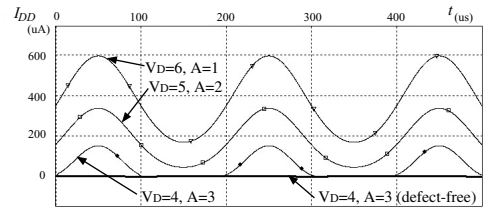
Table 1. The ratios of 2ω component to ω component at $f = 5kHz$



(a) defect(1), *f=5kHz, a=b=H*



(b) defect(2), *f=5kHz, a=b=H*



(c) defect(3), *f=5kHz, a=b=H*

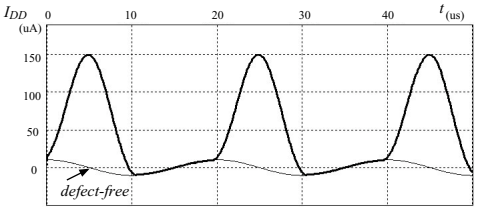
Figure 7. Measured waveforms of I_{DD}

The peak values of I_{DD}s in each defective DUT are at most a few times of that in the defect-free one, if the defective transistor conducts marginally. On the other hand, ratios of 2ω component to ω one in each defective DUT are much larger than those in the defect-free one. Hereafter, we call the ratio spectrum ratio. Table 1 shows spectrum ratios for the waveforms of Figure 7. The higher we select the value of A(the amplitude of $V_S(t)$), the more remarkable such a tendency becomes. This fact supports the results of the analysis described in the previous section that frequency analysis can detect such defects more sensitively than the conventional current test that the defective transistor conducts marginally.

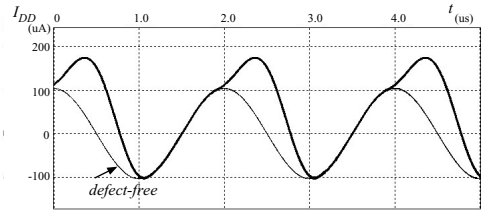
Figure 8 shows an example of the relation between I_{DD} waveform and frequency ω. Bold and thin lines are for defective and defect-free DUTs, respectively. The location of the defect is (3) of Figure 6. It is seen that the higher we select the frequency ω, the closer to a sinusoidal curve of frequency ω, the I_{DD} waveform is. Table 2 shows the spectrum ratios for them. These facts also support the results in the previous section.

5. Conclusion

In this study, we proposed one way to improve the detectability of our test method for CMOS floating gate defects which make transistors conduct marginally and showed that they can be detected more sensitively by analyzing the frequency spectrum of the supply current.



(a) *f=50kHz*



(b) *f=500kHz*

Figure 8. Influence of frequency ω on I_{DD} waveform

frequency	V_D	A	spectrum ratio	
			defective DUT	defect-free DUT
50kHz	4	3	0.499	0.012
500kHz	4	3	0.464	0.014

Table 2. Influence for the spectrum ratio

Our urgent work is to find a systematic way which can detect the floating gate defects as much as possible. Comparison of detectability in our method with that of the conventional I_{DDQ} test method and applicability check of our method for deep-submicron CMOS devices are also our important future works.

References

[1] W. Maly and P. Nigh, "Built-in Current Testing: Feasibility Study," Proc. of ICCAD, pp.340-343(1988).

[2] J. M. Soden and C. F. Hawkins, "Electrical Properties and Detection Methods for CMOS IC Defects," Proc. European Test Conf., pp.159-167(1989).

[3] M. Renovell and G. Gambon, "Electrical Analysis and Modeling of Floating Gate Fault,"IEEE Trans. CAD, vol.11,no.11, pp.1450-1458(1992).

[4] V. H. Champac, J. A. Rubio and J. Figueras, "Electrical Model of Floating Gate Defect in CMOS ICs : Implications on I_{DDQ} Testing," IEEE Trans. CAD, vol.13,no.3,pp.359-369(1994).

[5] M. Hashizume, M. Ichimiya, H. Yotsuyanagi and T. Tamesada, "CMOS Open Defect Detection by Supply Current Test, " Proc. of DATE2001, pp.509-513(2001).

[6] H. Michinishi, T. Yokohira, T. Okamoto, T. Kobayashi and T. Hondo, "CMOS Floating Gate Defect Detection Using I_{DDQ} Test with DC Power Supply Superposed by AC component, " Proc. of 11th Asian Test Symposium, pp.417-422(2002).